What is claimed is:

1.   A method for pulse modulation control of a switching regulator, the method comprising:

closing a total of m switches within a parallel series of m or more high side switches;

opening each high side switch when the output of the switching regulator reaches a first predetermined voltage or when the current through the m closed high side switches exceeds a predetermined limit;

closing a total of m low side switches within a parallel series of m or more low side switches; and

opening all low side switches when the output of the switching regulator falls below a second predetermined voltage.

2.   A method as recited in claim 1 where the switching regulator is selected from a group consisting of buck, boost and buck boost types.

3.   A method as recited in claim 1 which further comprises the step of opening all low side switches when a reverse current condition is detected within the switching regulator.

4.   A method as recited in claim 1 where the step of closing the high side switches is performed synchronously with a system clock and where the step of opening the high side switches is timed to occur no more than n cycles later.

5.   A method as recited in claim 4 where the steps of closing and opening the high side switches is controlled to avoid a predetermined switching frequency.

6.   A pulse modulation controller for a switching regulator, the controller comprising:

a parallel series of m or more high side switches;

a parallel series of m or more low side switches;

a controller configured to:

close a total of m switches high side switches;

open each high side switch when the output of the switching regulator reaches a first predetermined voltage or when the current through the m closed high side switches exceeds a predetermined limit;

close a total of m low side switches within a parallel series of m or more low side switches; and

open all low side switches when the output of the switching regulator falls below a second predetermined voltage.

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7.   A pulse modulation controller as recited in claim 6 where the switching regulator is selected from a group consisting of buck, boost and buck boost types.

8.   A pulse modulation controller as recited in claim 6 where the controller is configured to opening all low side switches when a reverse current condition is detected within the switching regulator.

9.   A pulse modulation controller as recited in claim 6 where the controller is configured to:

       close the high side switches synchronously with a system clock; and

       open the high side switches no more than n cycles later.

10.   A pulse modulation controller as recited in claim 9 where controller selectively skips one or more switching frequency bands when controlling the opening and closing of the high side switches.